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PATENT ABSTRACTS OF JAPAN

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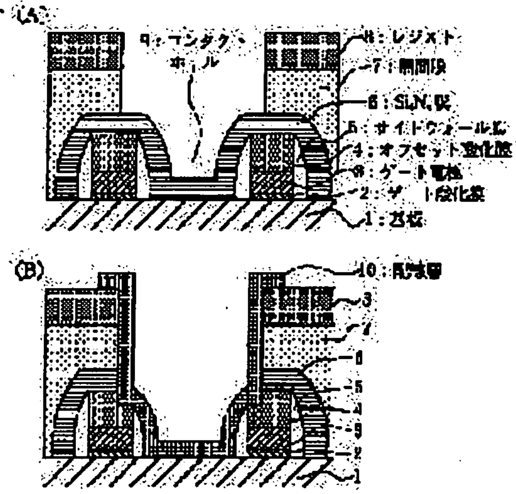
(54) DRY ETCHING METHOD

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a dry etching method for preventing a deterioration in interlayer breakdown strength in a wiring structure, and realizing a minute pattern of the wiring structure while the performance is not decreased even though an etching apparatus in a conventional SAC process in a semiconductor manufacturing process is used.

SOLUTION: In a dry etching method, an etching gas is fed to a reactive chamber and the etching is carried out by making the etching gas in a plasma state. As for the etching gas, an additive gas of NOx is added to a main gas containing C and F to use a mixed etching gas. When the interlayer film 7 is etched in a SAC manufacturing step, a selective ratio with a stopper of Si3M4 film 6 can be increased, and when a wiring layer 10 is formed, interlayer breakdown strength with a gate electrode 3 can be made sufficiently well.



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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the dry etching approach used in a semi-conductor manufacture process. It is related with the dry etching approach which plasma-izes etching gas and etches an oxide film in more detail.
[0002]
[Description of the Prior Art] In the semi-conductor manufacture process, SAC (Self Aligned Contact) which forms a contact hole in an interlayer film in order to connect a vertical wiring layer, carries out the laminating of the metal membrane, carries out etchback of this, and forms contact is used.
[0003] Drawing 3 is the process explanatory view of the conventional SAC processing process, and (B) of (A) is a sectional view at the time of wiring layer formation at the time of contact formation. Gate oxide 22 is formed according to a diffusion layer on the Si substrate 21, and the gate electrode 23 is formed on it. Furthermore, the offset oxide film 24 is formed with a CVD method on it.
[0004] In the side face of these gate oxide 22, the gate electrode 23, and the offset oxide film 24, it is LDD. The sidewall film 25 is formed by the dry cleaning dirty method, after depositing an oxide film with a CVD method. On these, Si3N4 film 26 which serves as a stopper of etching at the time of SAC processing is formed with a CVD method, and an interlayer film 27 is formed with a CVD method on it. Patterning of the resist 28 is carried out on said interlayer film 27 in the magnitude of 0.4 micrometers of diameters of contact on it. A contact hole 29 is formed in an interlayer film 27 by anisotropic etching by using as a mask said resist 28 which carried out patterning. A resist 28 is exfoliated with the oxygen plasma etc. after that, and SAC is formed by carrying out etchback of the whole wafer surface, for example, a wiring layer 30 is formed with a CVD method.
[0005] In such a SAC processing process, when 1300W were performed for the magnitude of 40mTorr (s) and impression RF power and etching was performed [the pressure in equipment / etching gas] for for example, C4F 8:18 sccm+CO:300 sccm+Ar:400sccm and a lower electrode on 35-degree C conditions, using for example, a magnetron mold plasma etching system as etching conditions for an interlayer film 27, for the etch rate, 450nm and homogeneity was [the selection ratio with 3Nfor Si4 film (shoulder)] 12.8 3.3%.
[0006]
[Problem(s) to be Solved by the Invention] However, in the dry etching approach in the above-mentioned conventional SAC processing, the selection ratio of 3Nfor Si4 film 26 at the time of etching an interlayer film 27 is small, and as shown in drawing 3 (A), the shoulder K of Si3N4 film 26 is etched, and it becomes thin. For this reason, in case a wiring layer 30 is formed after carrying out etchback of this Si3N4 film 26 and removing it, a sidewall 25 is greatly etched with the offset oxide film 24, and as shown in this drawing (B), the shoulder J of a sidewall 25 becomes thin. Consequently, pressure-proofing between layers between the gate electrode 23 and a wiring layer 30 deteriorates. Such pressure-proofing between layers is a property important also among the properties of a semiconductor device, and the dependability of a semiconductor device falls by the degradation.

[0007] This condition is further explained using drawing 4 . When over-etching of an interlayer film 27 is made into 30%, the amount of over-etching concerning the C section of Si3N4 film 26 turns into an amount which deducted B from the amount of etching which carries out over-etching 30% to A of drawing.
[0008] Therefore, selection ratio R to the C section of Si3N4 film 26 Thickness of R= (the amount of over-etching concerning the C section) / Si3N4 film It is set to = (Ax1.3-B)/C. According to this selection ratio, the shoulder C of Si3N4 film is etched greatly. Thus, the reason the shoulder of Si3N4 film is etched greatly is considered because there are few amounts of formation of the protective coat to an Si3N4 film top. On the conventional etching conditions, while scavenging as COF F which acts as etchant in etching gas by CO and suppressing the operation to Si3N4 film, the protective coat containing many C is formed on this Si3N4 film. However, with conventional etching gas, since F is removed only by CO, the removal effectiveness of F is considered that small protective coat sufficient on Si3N4 film is not formed.
[0009] In order to lessen the amount of etching of the shoulder of such Si3N4 film, it is possible to form a protective coat thickly and to perform anisotropic etching. Although it is possible for that to increase CO which has an operation of protective coat deposition in etching gas, if an operation of deposition is strong and increases CO, a protective coat will be formed superfluously, the omission nature of a contact hole will deteriorate, and this CO results in causing an etching stop. Therefore, it was very difficult to lessen the amount of etching of a shoulder and to form a detailed contact hole by anisotropic etching.
[0010] This invention prevents degradation of the pressure-proofing between layers of wiring structure, without spoiling the engine performance in consideration of the above-mentioned conventional technique using the etching system used by SAC processing of the usual semi-conductor manufacture process, and aims at offer of the dry etching approach that detailed-ization of wiring structure can be attained.
[0011]
[Means for Solving the Problem] In the dry etching approach which introduces etching gas into a reaction chamber and etches by plasma-izing this etching gas in this invention in order to attain said purpose, the gas containing C and F is made into the main gas as said etching gas, and the dry etching approach characterized by mixing and using the addition gas as which a general formula is expressed in this main gas by NOX is offered.
[0012] According to this configuration, by added NOX, an operation of F of etchant is suppressed, for example, the selection ratio to the stopper of Si3N4 film is raised, the amount of etching of the shoulder of this Si3N4 film is controlled, and micro processing becomes possible by anisotropic etching.
[0013] In the desirable example of a configuration, said NOX is NO. With this configuration, by adding NO, the selection ratio to the stopper of for example, Si3N4 film is raised, the amount of etching of the shoulder of this Si3N4 film is controlled, and micro processing becomes possible by anisotropic etching.

[0014] In another desirable example of a configuration, said NOX is NO2. With this configuration, by adding NO2, the selection ratio to the stopper of for example, Si3N4 film is raised, the amount of etching of the shoulder of this Si3N4 film is controlled, and micro processing becomes possible by anisotropic etching.
[0015] As for the dry etching approach of this invention, it is [therefore] effective to apply to SAC processing in a semi-conductor manufacture process. In this invention Form a gate electrode on a substrate and a wrap oxide film is formed for this gate electrode. In the etching approach used in the semiconductor device manufacture process which forms an interlayer film through Si3N4 film on this oxide film, etches this interlayer film and forms a contact hole The dry etching approach which makes the gas containing C and F the main gas as etching gas, and is characterized by mixing and using the addition gas as which a general formula is expressed in this main gas by NOX is offered. By this configuration, when etching an interlayer film in a SAC manufacture process, the amount of etching of Si3N4 film is stopped, etching of a wrap oxide film is suppressed for a gate electrode, the thickness of an oxide film can fully be maintained, a gate electrode can be protected certainly, and pressure-proofing

between layers between wiring layers can fully be secured.
[0016]
[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained based on a drawing.
[0017] Drawing 1 is the process explanatory view of the SAC processing process by the operation gestalt of this invention, (A) is the sectional view of the semi-conductor when using the dry etching approach of this invention, and (B) is a sectional view when forming a wiring layer after that.
[0018] Gate oxide 2 is formed by the diffusion method on the Si substrate 1, and the gate electrode 3 is formed on it. Furthermore, the offset oxide film 4 is formed with a CVD method on it. In the side of these gate oxide 2, the gate electrode 3, and the offset oxide film 4, it is LDD. The sidewall film 5 is formed by the dry cleaning dirty method, after depositing an oxide film with a CVD method. On these, Si3N4 film 6 which serves as a stopper of etching at the time of SAC processing is formed with a CVD method, and an interlayer film 7 is formed with a CVD method on it. Patterning of the resist 8 is carried out on said interlayer film 7 in the magnitude of 0.4 micrometers of diameters of contact on it. A contact hole 29 is formed in an interlayer film 27 by anisotropic etching by using as a mask said resist 8 which carried out patterning. A resist 28 is exfoliated with the oxygen plasma etc. after that, and SAC is formed by carrying out etchback of the whole wafer surface, for example, a wiring layer 10 is formed with a CVD method.
[0019] Drawing 2 is the schematic diagram of the dry etching system when etching. This equipment is a magnetron mold dry etching system which introduces gas into a reaction chamber and etches by plasma-izing gas by high frequency.
[0020] This etching system is equipped with the up electrode 12 which has the gas inlet 11, and the lower electrode 15 which countered this up electrode 12 and has been arranged in a reaction chamber 18. The wafer 14 used as an etching object is carried on the lower electrode 15. RF generator 16 is connected to the lower electrode 15. The shield ring 13 is formed in the lower periphery of the up electrode 11 so that the lower electrode 14 may be surrounded. A permanent magnet 17 is arranged by the periphery part of the up electrode 11.
[0021] In such a configuration, introducing etching gas in a reaction chamber 18 from the gas inlet 11, by impressing high frequency by RF generator 16, etching gas plasma-izes and a wafer 14 is etched by this plasma.
[0022] When said SAC processing process was carried out using this etching system, the interlayer film 7 was etched on the etching conditions of the following conditions 1 and 2.
[0023] condition 1 equipment internal pressure: -- 40mTorr impression RF power: -- 1300W etching gas: -- main -- gas:C4F 818 sccm+CO200 sccm+Ar400sccm addition gas: -- NO50sccm lower electrode temperature: -- when 35 degrees C was etched on this condition, 437 nm/min and homogeneity was [the selection ratio of the etch rate of 3Nfor Si4 film (shoulder)] 14.2 3.8%.
[0024] Thus, by mixing NO as addition gas as etching gas in the main gas which consists of C4F8, and CO and Ar, the selection ratio of 3Nfor Si4 film was able to be enlarged, the amount of etching of the shoulder of Si3N4 film was able to be stopped, and precise anisotropic etching was able to be performed.
[0025] condition 2 equipment internal pressure: -- 40mTorr impression RF power: -- 1300W etching gas: -- main -- gas:C4F 818 sccm+CO200 sccm+Ar400sccm addition gas: -- NO250sccm lower electrode temperature: -- when 35 degrees C was etched on this condition, 432 nm/min and homogeneity was [the selection ratio of the etch rate of 3Nfor Si4 film (shoulder)] 13.7 4.2%.
[0026] Thus, by mixing NO2 as addition gas as etching gas in the main gas which consists of C4F8, and CO and Ar, the selection ratio of 3Nfor Si4 film was able to be enlarged, the amount of etching of the shoulder of Si3N4 film was able to be stopped, and precise anisotropic etching was able to be performed.
[0027] In addition, the gas which replaces with C4F8 of the main gas, and is expressed with other CXFY(s) or CXHYFZ(s) may be used, and it may replace with CO and COO2 [2] may be used.
[0028] Moreover, as an interlayer film, it is SiO2. BPSG or PSG can be used.

[0029]
[Effect of the Invention] As explained above, in this invention, by NOX added to etching gas, an operation of F of etchant is suppressed, for example, the selection ratio to the stopper of Si3N4 film is raised, the amount of etching of the shoulder of this Si3N4 film is controlled, and micro processing becomes possible by anisotropic etching. Thereby, when performing SAC processing of a semiconductor device, etching of the sidewall which protects a gate electrode can be controlled, pressure-proofing between layers between wiring layers, such as aluminum wiring, can be secured enough, and the dependability of wiring structure can be raised.
[0030] Moreover, since addition gas is gas by which work of cleaning contains strong O to the deposit in a reaction chamber, it can press down the dirt in a reaction chamber. Furthermore, ashing and washing after forming the contact hole of SAC processing can also be made easy.

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CLAIMS

[Claim(s)]
[Claim 1] The dry etching approach which introduces etching gas into a reaction chamber, makes the gas containing C and F the main gas as said etching gas in the dry etching approach which etches by plasma-izing this etching gas, and is characterized by mixing and using the addition gas as which a general formula is expressed in this main gas by NOX.
[Claim 2] Said NOX is the dry etching approach according to claim 1 characterized by being NO.
[Claim 3] Said NOX is the dry etching approach according to claim 1 characterized by being NO2.
[Claim 4] Form a gate electrode on a substrate and a wrap oxide film is formed for this gate electrode. In the etching approach used in the semiconductor device manufacture process which forms an interlayer film through Si3N4 film on this oxide film, etches this interlayer film and forms a contact hole The dry etching approach which makes the gas containing C and F the main gas as etching gas, and is characterized by mixing and using the addition gas as which a general formula is expressed in this main gas by NOX.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] (A) is a sectional view when it is the sectional view of the semi-conductor when using the dry etching approach of this invention and (B) forms a wiring layer after that.
[Drawing 2] The schematic diagram of the dry etching system when etching
[Drawing 3] It is the manufacture approach of the conventional semiconductor device, and, for (A), (B) is a sectional view at the time of wiring layer formation at the time of contact formation.
[Drawing 4] The sectional view when carrying out dry etching of the interlayer film.
[Description of Notations]
1: A substrate, 2:gate oxide, 3:gates electrodes, 4 : an offset oxide film, 5:LDD A sidewall, 6:Si3N4 film, 7:interlayer film, 8:resist, 9:contact hole, 10:wiring layer, 11:gas inlet, a 12:up electrode, 13:shield ring, 14:wafer, a 15:lower electrode, 16:RF generator, 17: Permanent magnet.

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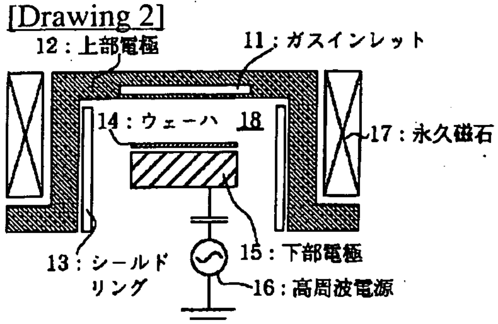
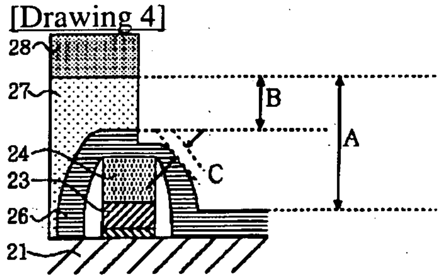
DRAWINGS

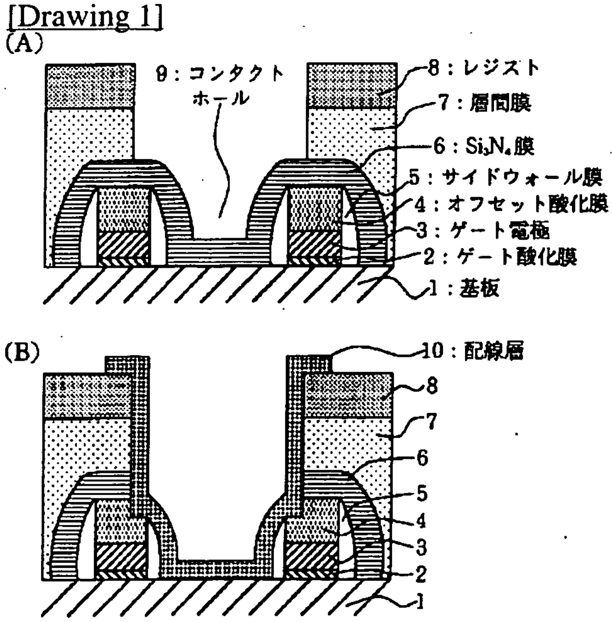
[Drawing 2]



[Drawing 4]



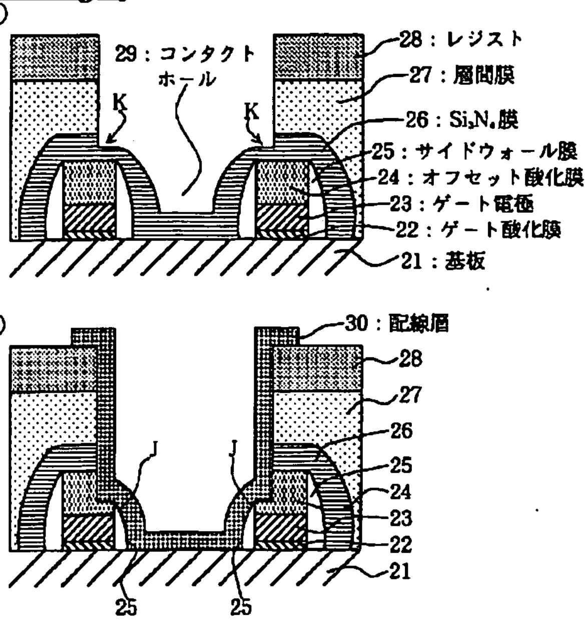
[Drawing 1]



[Drawing 3]

(A)

(B)



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